I Claim:

1. A method of testing a subject integrated circuit (IC) package comprising:

mounting the subject IC package on a subject printed circuit board (PCB);

removably connecting the subject PCB to a motherboard along with a plurality of other PCBs having other IC packages mounted thereon;

exposing the subject IC package, the subject PCB, the other IC packages and the other PCBs to thermally varying test conditions;

monitoring the subject IC package and the other IC packages for a test failure during exposure to the thermally varying test conditions;

determining whether the subject IC package has experienced the test failure;

upon determining that the subject IC package has experienced the test failure, removing the subject PCB from the motherboard; and

performing an electrical test on the subject IC package to determine a location of the test failure.

2. A method as defined in claim 1 further comprising:

removably connecting the subject PCB to the motherboard by edge card connection.

3. A method as defined in claim 2 wherein:

the subject PCB has edge card connectors on only one edge.

4. A method as defined in claim 1 further comprising:

removing the subject PCB from the motherboard without altering the motherboard.

5. A method as defined in claim 1 further comprising:

continuing the exposing and monitoring of the other IC packages and the other PCBs while electrically testing the subject IC package.

6. A method as defined in claim 1 further comprising:

returning the subject PCB to the motherboard to resume the exposing and monitoring of the subject IC package and the subject PCB.

7. A method of testing integrated circuit (IC) packages comprising:

mounting the IC packages on printed circuit boards (PCBs);

connecting the PCBs to a motherboard;

applying test signals to the IC packages through the motherboard and the PCBs;

subjecting the IC packages to thermal cycling;

monitoring the test signals during the thermal cycling to determine whether any of the IC packages exhibit a failure condition;

upon determining that one or more IC packages exhibit the failure condition, removing from the motherboard the PCBs to which the one or more IC packages are mounted; and

performing an electrical test on each of the one or more IC packages to determine a location of the failure condition.

8. A method as defined in claim 7 further comprising:

placing the motherboard in a thermal test chamber in which the thermal cycling occurs.

9. A method of testing integrated circuit (IC) packages comprising:

mounting the IC packages on printed circuit boards (PCBs) each having edge connectors on only one edge;

removably connecting the PCBs to a motherboard perpendicular to the motherboard;

applying a test electrical bias to the PCBs and the IC packages for a period of time;

removing the PCBs and the IC packages from the motherboard; and

electrically testing the IC packages to determine whether any of the IC packages fail due to application of the test electrical bias.

10. A method as defined in claim 9 further comprising:

subjecting the motherboard, the PCBs and the IC packages to thermal and relative humidity test conditions.

11. A method as defined in claim 9 further comprising a highly accelerated stress test (HAST).

12. A method as defined in claim 9 further comprising:

placing the motherboard with the PCBs and the IC packages in a test chamber within which the test electrical bias is applied to the PCBs and the IC packages.

13. An integrated circuit (IC) package testing apparatus comprising:

a plurality of printed circuit boards (PCBs), each capable of supporting an IC package to be tested; and

a motherboard to which the PCBs are removably connected;

and wherein:

the motherboard, the PCBs and the IC packages are adapted to be placed in a thermal test chamber within which the motherboard, the PCBs and the IC packages are subjected to thermal cycling conditions while electrical signals are applied to the IC packages through the motherboard and the PCBs and monitored for a failure condition; and

the motherboard and the PCBs are adapted to be separated for electrical testing of the PCBs and the IC packages to determine a location of a cause of the failure condition.

14. An integrated circuit (IC) package testing apparatus as defined in claim 13 wherein:

the PCBs are connected substantially perpendicular to the motherboard.

15. An integrated circuit (IC) package testing apparatus as defined in claim 13 wherein:

the PCBs have edge card connections on only one edge connected to the motherboard.

16. An integrated circuit (IC) package testing apparatus as defined in claim 13 wherein:

the PCBs and the motherboard can be removably reconnected after being separated.

17. An integrated circuit (IC) package testing apparatus as defined in claim 13 wherein:

the motherboard is not damaged when the PCBs are separated therefrom.

18. An integrated circuit (IC) package testing apparatus comprising:

a plurality of printed circuit boards (PCBs), each having edge connectors on only one edge and each capable of supporting an IC package to be tested; and

a motherboard to which the PCBs are removably connected by edge card connection;

and wherein:

the motherboard, the PCBs and the IC packages are adapted to be subjected to electrical bias test signals; and

the motherboard and the PCBs are adapted to be separated for electrical testing of the PCBs and the IC packages to determine whether the electrical bias test signals caused a failure condition in any of the IC packages.

19. An integrated circuit (IC) package testing apparatus as defined in claim 18 wherein:

the PCBs are connected substantially perpendicular to the motherboard.

20. An integrated circuit (IC) package testing apparatus as defined in claim 18 wherein:

the motherboard, the PCBs and the IC packages are adapted to be subjected to a highly accelerated stress test (HAST).